Glass Substrate With Integrated Waveguides for Surface Mount Photonic Packaging

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(Invited Paper)

***Abstract*—Co-packaged optics in next-generation datacenters require the assembly of multiple components on the same multi-chip module (MCM) and interconnection with hundreds of optical fibers. A novel photonic packaging substrate is required to leverage high-throughput electronic assembly with high precision optical alignment. This report highlights the results of glass substrate optimization to include optical waveguides, a fiber connector, and chip interfaces, as well as features for electrical connectivity, as a potential component for a co-packaging solution. Glass with smooth surfaces and high precision alignment features enables surface mounted flip-chip assembly of electrical integrated circuits, photonic components, and optical fiber connectors. All components will be placed by vision alignment using precise fiducials or passive alignment in mechanical features to the surface of the glass substrate with optical and electrical interconnects. Flip-chip assembly of photonic components is enabled by evanescent coupling with couplers having a minimum non-linear taper length of 1.5 mm. The designed interface loss to the integrated ion-exchanged glass waveguides is less than 1 dB with an interface which is robust to lateral misalignment of up to 4 microns. Light can be transmitted in the glass substrate with a propagation loss of 0.1 dB/cm. Fiber interfaces are mechanically and thermally decoupled from the photonic component and glass waveguides can fan-out the component pitch from 50 to 250 microns of the MTP-16 ferrule connector. The solder reflow compatible connector receptacle is passively aligned and demonstrate with an average loss of 0.68 dB.**

***Index Terms*—Connectors, multichip modules, optical coupling, optical waveguides, silicon photonics, surface mount technology.**

I. Introduction

THE capacity of switch Application Specific Integrated Circuits (ASICs) in datacenters has experienced exponential growth over time, having doubled every two years in the last decade. The current switch generation has a bandwidth of 12.8 Tb/s and 32 ports of 400 Gb/s [1]. A switch ASIC module is typically assembled on a printed circuit board (PCB) inside a single rack unit form-factor. Electrical high-speed signals are routed to the pluggable optical transceivers located at the front-panel, many centimeters away. The limiting factors for next generation switches are the required power to drive the electrical signals across a PCB and the front panel density for the optical modules [2]. Reducing the length of the electrical lines by replacing the optical modules at the front panel with optical connectors and integrating the transceiver components to the switch package will decrease the electrical path length to millimeters. Currently, the work on such complex multi-chip modules (MCM) is in the development stage [3]. In addition to the challenge of interconnecting the optical transceiver I/Os with optical fibers, additional packaging challenges are the co-design of signal and power distribution, thermal management, and mechanical support. For co-packaged optics, the switch ASIC located in the center of the module will be surrounded by the transceivers which are connected to an array of optical fibers. One scenario for a next generation 51.2 Tb/s switch ASIC is the assembly of sixteen 3.2 Tb/s photonic integrated circuits (PICs), each with sixteen fibers (eight 400 Gb/s transmitter and eight 400 Gb/s receiver channels) resulting in 256 optical fibers going to the front panel. Today, optical modules are electrically assembled first, followed by active optical alignment of a fiber array unit (FAU) or passive placement of a fiber array in precisely etched V-grooves [4] which is bonded using a UV-curing adhesive. Alternatively, initial work has been done on solder-reflow compatible fiber-to-chip interconnects to change the order of the process sequence for photonic ball grid array (BGA) package to PCB assembly [5]. High-density integrated (HDI) organic laminates for MCMs were demonstrated with dimensions of 90 mm $\times$ 90 mm [6]. A similar size would be required for co-packaged optics.

This work explores an optoelectronic glass substrate with optical interconnects, electrical redistribution layers (RDLs), and through glass vias (TGVs) that can enable the high-throughput pick-and-place assembly of electrical and photonic ICs as shown in the schematic cross-sectional view in Fig. 1. Specifically, experimental results are reported for a glass substrate incorporating a) waveguides optimized to have low propagation loss; b) MTP-16 fiber connector interface with passive alignment; c) a cavity with through-glass vias interconnecting the substrate sides. Design and simulation results are also reported for an optical interface connecting glass and silicon photonic chip waveguides. While each of these components is studied

Manuscript received July 15, 2020; revised September 16, 2020; accepted October 12, 2020. Date of publication October 23, 2020; date of current version February 16, 2021. *(Corresponding author: Lars Brusberg.)*

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Digital Object Identifier 10.1109/JLT.2020.3033295

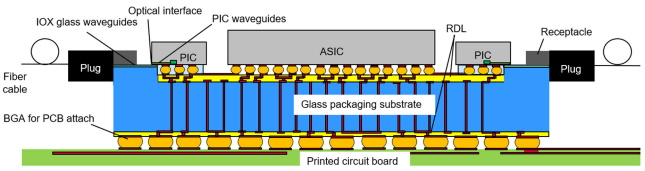

Fig. 1. Glass substrate with optical waveguides and electrical interconnects for surface mount assembly of application specified integrated circuit (ASIC), photonic integrated circuits (PIC) and fiber connectors.

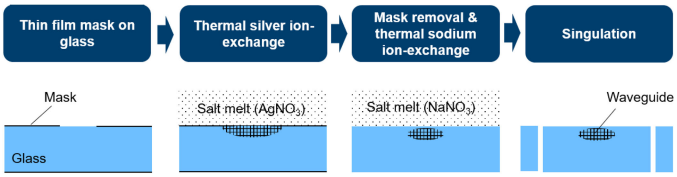

Fig. 2. Glass waveguide process consists of multiple process steps including thin film mask, ion-exchange and laser singulation.

separately in this work, altogether they form a basis for realizing the co-packaging concept depicted in Fig. 1. The optical and electrical interface interconnection for each transceiver occur in a single assembly step. The optical interface consists of an evanescent coupler between the silicon photonics chiplet and the glass waveguides integrated in the substrate. Glass waveguides are interconnected to optical fibers via an optical fiber array connector. The length of the glass waveguides could be extended all the way to the front-panel to replace fiber fly-overs.

II. Glass Waveguides

Thermal ion-exchange [7] is a batch process where multiple glass sheets can be processed in parallel for scalability and lowest cost. The fabrication of ion-exchange optical waveguides in 150 mm alkali containing aluminosilicate glass wafers was accomplished by performing multiple processing steps. These steps can be categorized into four groups being (1) lithography, (2) primary silver ion-exchange, (3) fiducial protection, mask removal and secondary ion-exchange, and (4) Laser singulation. The process flow is schematically shown in Fig. 2.

The singulation of the glass substrate was achieved using Corning's ultrafast laser nanoPerforation cutting process [8]. The laser modification regions were controlled to avoid damaging the ion-exchange waveguide regions. A mechanical force or, in some cases, CO_2 laser irradiation was applied to separate the substrate along the defined nanoPerforated line. The resulting waveguide end-faces (Fig. 3) enabled low-loss optical edge coupling without additional post-processing steps (e.g., polishing) to smooth the surface.

The flexibility of the process is further demonstrated in the free-form laser cutting of a 150 mm wafers into many different sample sizes as shown in Fig. 4.

Two waveguide designs were fabricated and tested: one with a peak refractive index increase of 0.0047 and another with a higher index contrast (0.0093) to further confine the mode to enable tighter waveguide bends. The cut-back method was

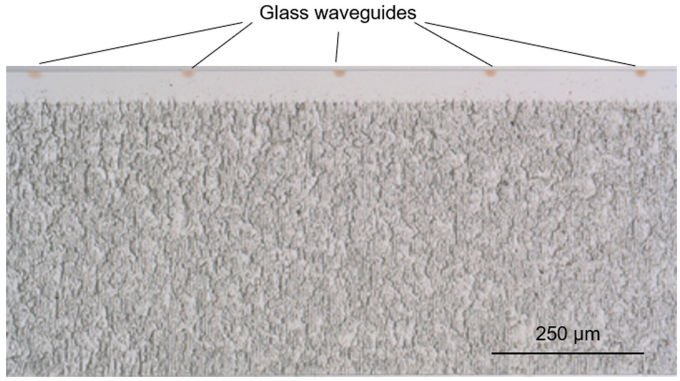

Fig. 3. Corning Laser Technologies nanoPerforation glass cutting process for optical waveguide end faces. Waveguide array with 250 μm is located below the top surface of the glass.

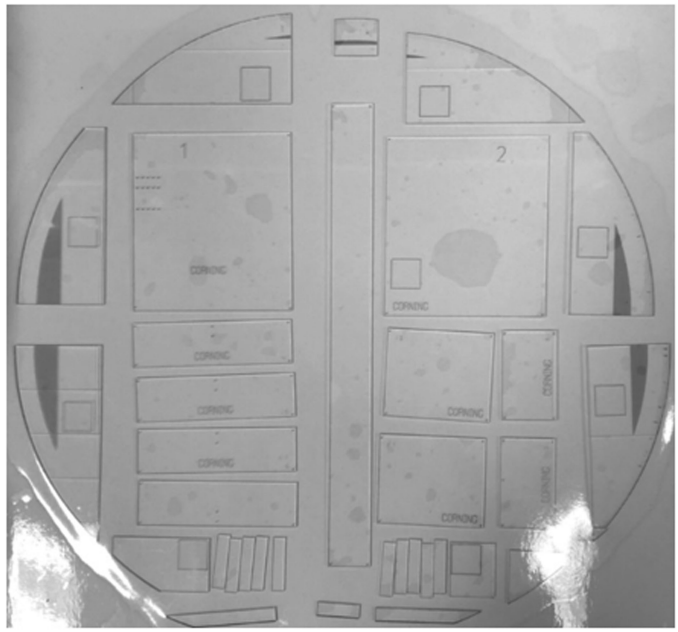

Fig. 4. Multi-project 150 mm diameter glass waveguide wafer with samples of different sizes.

employed with single-mode fiber launch and detection index-matched interfaces yielding waveguide propagation losses of 0.08 dB/cm and 0.11 dB/cm at 1310 nm wavelength for the low- and high-index contrast waveguides, respectively. The cross-section of the waveguide profile was measured with refractive near field (RNF) method [9]. The refractive index profiles for the low-index (Fig. 5) and high-index (Fig. 6) contrast waveguides resulted in a per facet coupling loss to single-mode optical fiber of 0.3 dB and 0.6 dB at 1310 nm wavelength, respectively.

As a result of the low index contrast, the bend loss increased exponentially for bend radii smaller than 30 mm for the low index contrast design. In contrast, the higher index contrast design results in lower bend losses and a smaller minimum bend radius of 10 mm. Simulations revealed <-60 dB cross-talk for two parallel 3 mm long waveguides separated by 50 μm.

Fig. 7 shows a waveguide layout for interconnection between a PIC and three MTP-16 ferrule fiber connectors. The PIC

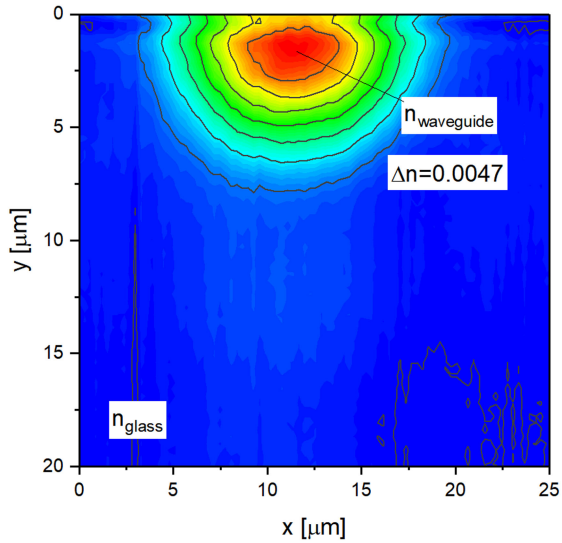

Fig. 5. Measured refractive index cross-section of the low-index contrast single-mode glass waveguide. The graded index waveguide is next to the glass surface (y=0) with index maximum of 0.0047 represented by the red area. The bulk glass is represented in blue.

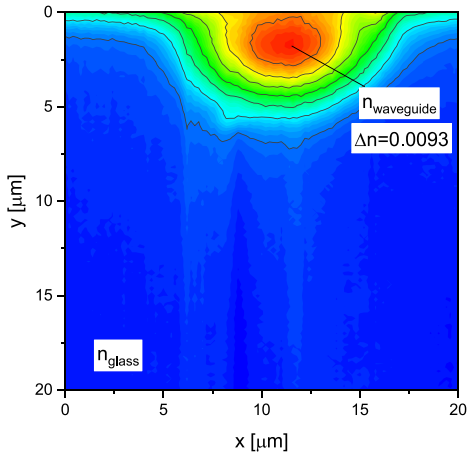

Fig. 6. Measured refractive index cross-section of the higher-index contrast single-mode glass waveguide. The graded index waveguide is next to the glass surface (y=0) with index maximum of 0.0093 represented by the red area. The bulk glass is represented in blue.

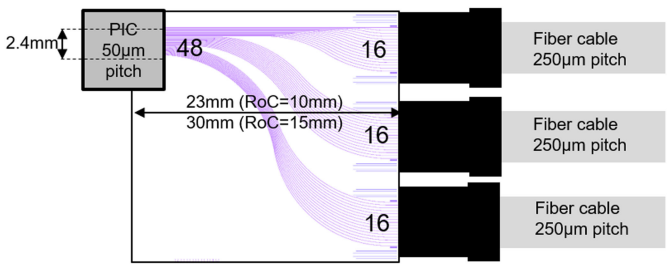

Fig. 7. Layout for the waveguide fan-out between the PIC and the fiber connectors with RoC=10 mm or RoC=15 mm.

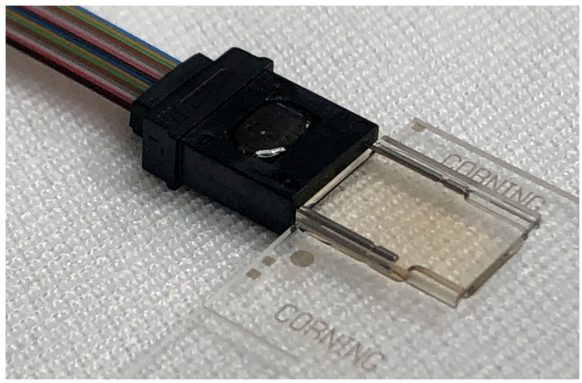

Fig. 8. Fiber MTP-16 ferrule connector with passively aligned pins on a glass substrate.

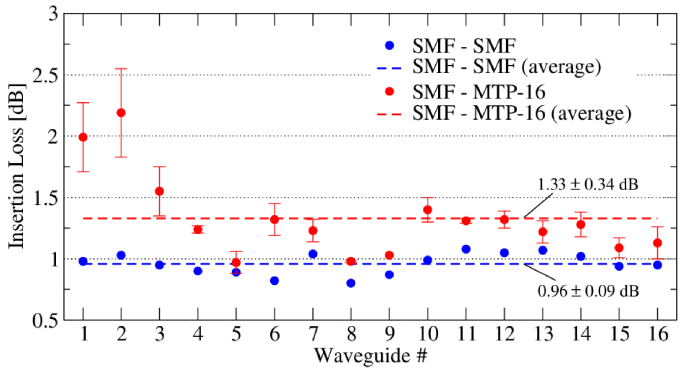

Fig. 9. Measured insertion loss at 1310 nm wavelength for fiber probing both sides (SMF – SMF) and with mated connector on one side (SMF - MTP-16).

has 48 waveguides with a 50 μm pitch. Each MTP-16 ferrule connector has 16 fibers with a 250 μm pitch. The interconnecting waveguide fan-out has a radius of curvature (RoC) of 10 mm. A second similar design was made with RoC of 15 mm. Both designs were fabricated with the higher index contrast waveguide design. The waveguide loss was measured to be in the range 0.3 dB to 1 dB at a wavelength of 1310 nm without coupling loss.

III. Fiber MTP-16 Connector Interface

Glass waveguides were end-coupled with standard MTP-16 connectors which have alignment pins with 550 μm in diameter. A single row of a 2-row MTP-16 ferrule was populated with fibers to allow an offset between the fibers and the guide pins. Laser cut optical end-faces and laser ablated features in the glass for passive pin alignment were made before the two guide pins were assembled to the glass waveguide substrate. The pins were locked in place with a top lid by an adhesive. The assembled fiber receptacle and mated MTP-16 ferrule connector is shown in Fig. 8.

The average reference insertion loss was 0.96±0.09 dB for 16 waveguides all fiber probed from both sides at 1310 nm wavelength. The data is summarized in Fig. 9. The reference

insertion loss of the glass waveguide sample includes mode-mismatch (∼0.31 dB per waveguide facet and waveguide propagation loss (∼0.1 dB/cm). Both fibers were actively aligned, and we assume no additional loss due to fiber misalignment. Then, MTP-16 jumper cables were mated on the pin side. The same sample was remeasured using single-mode fiber probing on the waveguide output side. The average insertion loss was 1.33±0.34 dB resulting in an average fiber misalignment loss of 0.37 dB after subtracting the reference insertion loss. The single-mode fiber mismatch adds 0.31 dB for a total average connector coupling loss of 0.68 dB. All measurements were done with index-matching fluid between fiber and waveguide end-facet. MTP-16 jumper cables were made with multimode 2x16 MTP-16 ferrules which come with non-angled end-faces and the required offset of each fiber row to the center of the pins. The connector loss variation between different jumpers can be explained by the core position variation between the single-mode fiber (SMF) position inside the multimode MTP-16 ferrules.

The difference between the coefficient of thermal expansion of the glass (∼8 ppm/K) and the thermoplastic PPS MT ferrule (∼16 ppm/K) can lead to a lateral fiber misalignment of up to 1.4 microns causing additional loss of 0.4 dB across a temperature range of 20 °C to 110 °C. Reducing the operation temperature range to $\Delta T = 45$ °C reduces the additional misalignment loss to 0.1 dB. Hybrid injection-molded ferrules [10] with matched CTE would mitigate the additional misalignment loss across the operating temperature range.

IV. Evanescent PIC Coupler

Edge and grating couplers are two common methods of interfacing between fiber and on-chip waveguide modes [11]. Recently, evanescent coupling methods (also referred to as adiabatic couplers when used with slowly tapered waveguides) that use an intermediary polymer waveguide interposer to connect fiber modes to on-chip waveguide modes have been demonstrated [12–14]. Such an approach is scalable to high optical port counts and can be automated by pick and place machines.

As an alternative to the polymer waveguide interposer, the optical quality of the top surface of a glass substrate hosting ion-exchanged (IOX) waveguides makes it well suited for evanescent mode coupling to PIC waveguides. Initial design work showed a coupling loss of 0.1 dB for a taper length of 2.6 mm [15]. Fig. 10 illustrates the transverse cross-section of the coupler, in which a Si-waveguide is formed on a buried oxide layer of a silicon-on-insulator wafer and covered by a thin SiO2 layer. The Si-stack is flip-chip bonded on top of the glass substrate, with IOX and Si waveguides aligned. The optically transparent adhesive between the glass and the Si-chip top surface provides mechanical contact and controls the waveguide separation.

Eigen-mode expansion method was employed to evaluate the evanescent coupling between a 450 nm x 220 nm Si-waveguide mode and the IOX waveguide mode for the nominal parameters shown in Fig. 10. Intrinsic material absorption and radiative propagation losses are accounted for in the model, except for the radiative loss due to the finite thickness of the buried oxide (BOX) layer, whose impact is analyzed separately. Scattering loss due to the Si-waveguide non-uniformities induced by the lithography and etching processes was not considered in the optical loss estimate.

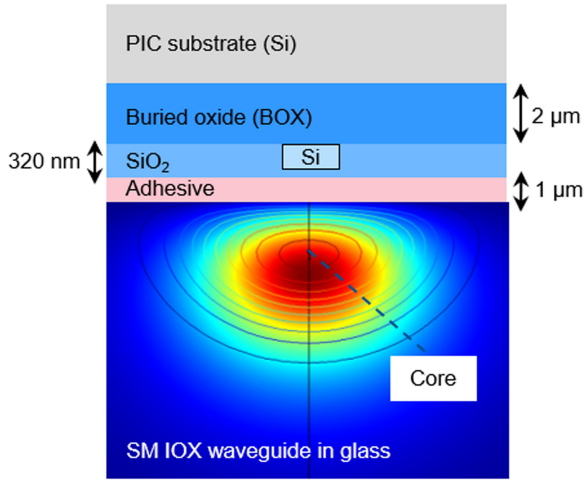

Fig. 10. Cross-section view (not to scale) of an ion-exchange (IOX) glass – Si-waveguide stack for evanescent coupling. The color plot shows the electrical field distribution of the single-mode ion-exchange waveguide which is overlapped with the contour lines of the refractive index gradient with an index delta of 0.0047 at the core position.

Low-loss power transfer between Si and glass-waveguides was achieved by adiabatically tapering the Si-waveguide width down to 120 nm. The tapering was made in two stages to reduce the total taper length [16]. In the first stage, the Si waveguide width is reduced from 450 nm to 250 nm by using a mode-converter of length 100 μm [17]. During this stage, the effective refractive index of the super-mode localized predominantly in the Si waveguide is reduced without significant power transfer to the IOX waveguide. In the second stage, the Si waveguide width is varied from 250 nm to 120 nm, and efficient transfer of TE (TM) mode power occurs at Si widths around 176 (138) nm, with the super-mode fully localized in the IOX waveguide when the taper width reaches 120 nm. Design of the evanescent coupling region was made by calculating consecutive super-mode overlap integrals along the taper as a measure of mode-mismatch loss variation [18]. The taper shape (i.e., width length) is obtained by enforcing a constant mode-mismatch loss along the taper length. The taper design was made taking into consideration the super-mode overlap integrals for both TE and TM modes.

C-band Si-waveguide tapers designed for coupling to the single-mode IOX waveguide using this approach can theoretically achieve <0.5 dB (<1 dB) loss for the TE (TM) mode when coupler length L_c >1 mm and under nominal alignment conditions, as shown in Fig. 11(a). For the TE (TM) mode less than 1 dB (2.5 dB) increase in loss was computed across the 1525–1585 nm wavelength range. With up to 4 μm lateral offset the loss remains below ∼1 dB for $L_c = 1.5$ mm for both TE and TM modes as shown in Fig. 11(a–b). Ripples in the loss dependence on the taper length [Fig. 11(a)] lead to the crossing of the loss vs offset curves for different taper lengths in Fig. 11(b).

The sensitivity of the coupling loss to the separation between the waveguides, and hence to the adhesive layer thickness,

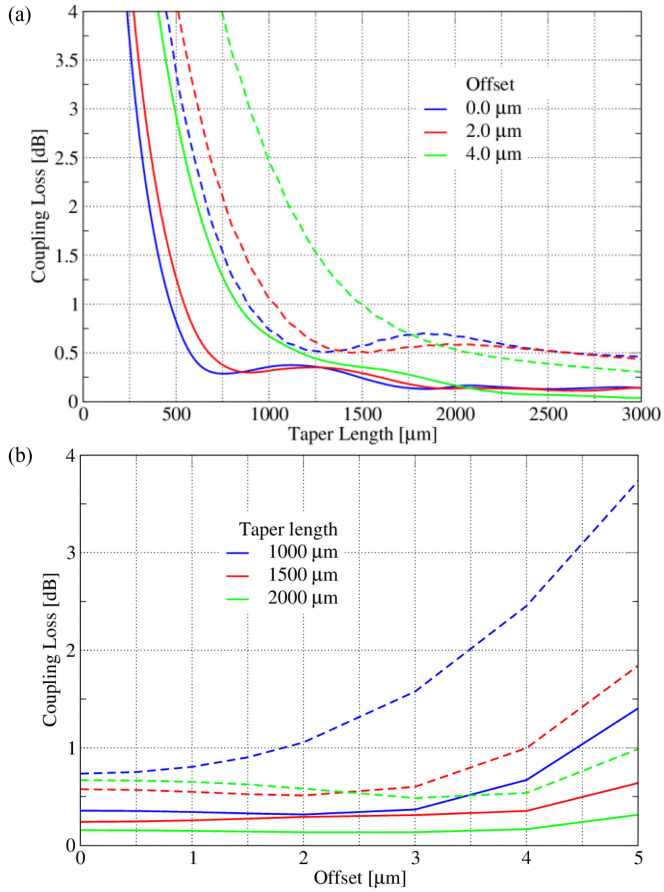

Fig. 11. Coupling loss dependence on the lateral misalignment of the Si- and glass-waveguide at 1550 nm wavelength for TE (solid) and TM (dashed) modes for (a) varying evanescent taper (stage two) length, (b) varying offset values.

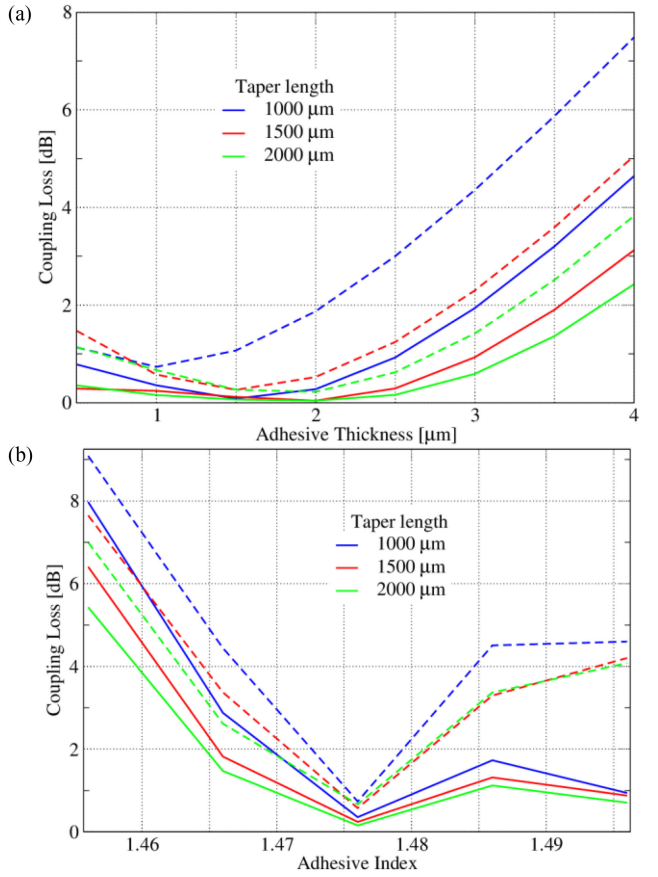

Fig. 12. Coupling loss dependence on the (a) adhesive layer thickness and (b) refractive index, for taper lengths Lc=1000–2000 μm.

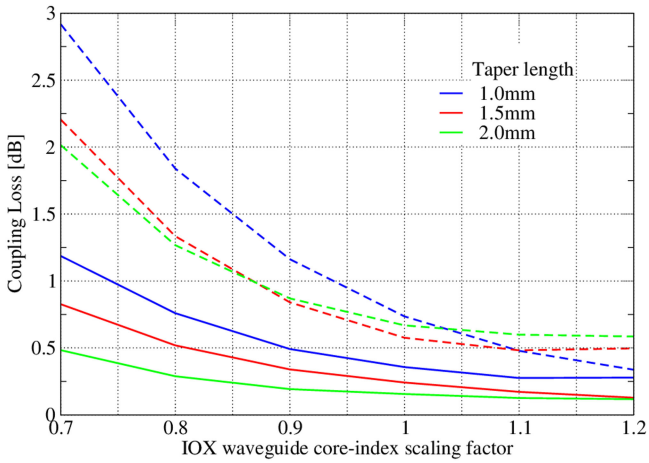

Fig. 13. Coupling loss dependence on the glass waveguide core index contrast (scaling factor of 1 corresponds to the target design).

leads to sub-micron tolerances on the waveguide separation [Fig. 12(a)]. This is the main disadvantage of the evanescent coupling scheme, which otherwise is attractive in terms of vertical integration, low loss, relatively wide bandwidth and polarization control.

In addition to a stringent control of the adhesive bond-line thickness, stability of the cured adhesive refractive index in time and with respect to temperature changes is also required to maintain high coupling efficiency. Coupling loss is limited to $<$1 dB for changes in the refractive index of the adhesive on the order of $\sim 5 \times 10^{-3}$ [Fig. 12(b)]. The impact of IOX glass waveguide refractive index variation on the coupling loss is shown in Fig. 13, based on the core index change realized by scaling the target core refractive index contrast by a spatially constant scaling factor. Refractive index contrast reduction represented by scaling factors $<$1 represents approximately the diffusion of IOX waveguide core over lifetime and thus should be limited to less than $\sim$15% to keep the loss for both TE and TM polarizations below 1.5 dB. In addition to the IOX waveguide core index variation, the overall glass index change can also cause an increase in the coupling loss: glass index reduction of 3×10^{-3} (e.g., due to increase in operating temperature) can lead to $\sim$1dB additional loss, and therefore should be considered during coupler design.

When the Si-waveguide width is reduced along the taper, the resulting increase in the mode size of the glass-Si waveguide super-mode is accompanied by an enhanced radiative loss due to the coupling to the high-index Si substrate through the BOX layer, adding to the coupling losses discussed above. Fig. 14 shows this dependence computed for 2$-$3 μm thick BOX layers. The radiative loss is seen to be $<$2 dB/cm when the optical mode

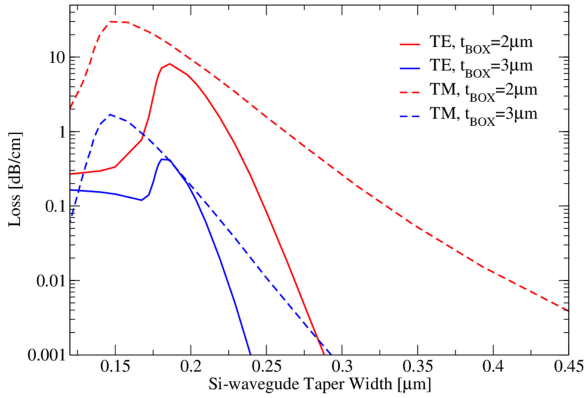

Fig. 14. Radiative loss dependence on the Si-waveguide width computed for 2 and 3 μm BOX layer thickness.

is confined almost fully in either the Si waveguide (for Si taper widths >250 nm), or in glass waveguide (for Si taper widths <120nm). The loss increases significantly to >5 dB/cm for TE mode (>10 dB/cm for TM mode), in a section of the taper over which power transfer from one waveguide to another takes place.

Simulation results also indicate more than an order of magnitude reduction in the radiative loss for 3 μm BOX layer, as further means to reduce its impact. The integrated loss over the length of the coupler is estimated to be ~0.5 dB (2.7 dB) for TE (TM) mode with 2 μm thick BOX layer and $L_c = 1500$ μm. Increasing BOX layer thickness reduces this source of radiative loss to <0.04 dB for TE mode and <0.15 dB for TM mode.

V. Glass Packaging Substrate

Near-term forecasts indicate the continued drive toward reduced channel pitch, increased baud rates, and multi-layer electrical routing which all lead to increased complexity/precision/cost. With serial electrical line rates for 51.2 Tb/s switches expected to increase from 56 Gb/s to 112 Gb/s per lane, heterogenous integration of switch ASICs and PIC transceivers onto a common package substrate reduces the electrical interconnect loss by decreasing the required reach from at least 100 mm across the PCB to the front panel to ≤50 mm across the substrate package. The decreased reach helps counteract the effects of the higher electrical loss at the doubled Nyquist frequency and is expected to reduce the link power budget by ~20%. However, there are significant electrical, thermal and mechanical packaging challenges particularly resulting from substrate sizes approaching 90 mm × 90 mm for co-packaged optics. New materials and assembly approaches are needed for: low loss and power efficient high-speed electrical interconnects; thermal management of a high-power consuming ASICs on the same substrate as temperature sensitive PICs; low substrate warpage, and high electrical reliability of chip-to-package substrate bumps/pillars and substrate-to-board ball grid array (BGA). Glass has a unique combination of properties [19] that well-position it for these co-packaging challenges.

Our approach consists of a single glass substrate where the top redistribution lines (RDLs) connect high speed electrical lanes between the ASIC and the optical transceivers along with

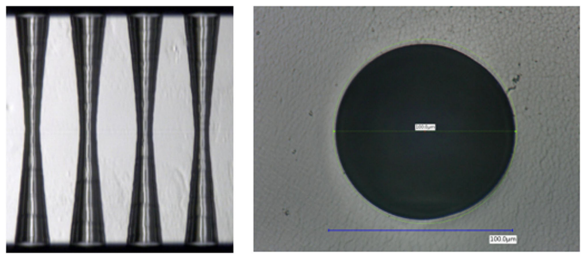

Fig. 15. Cross-section (left) and top (right) view of through glass vias in 0.6 mm glass with 150 μm TGV pitch and entrance diameter of 100 μm

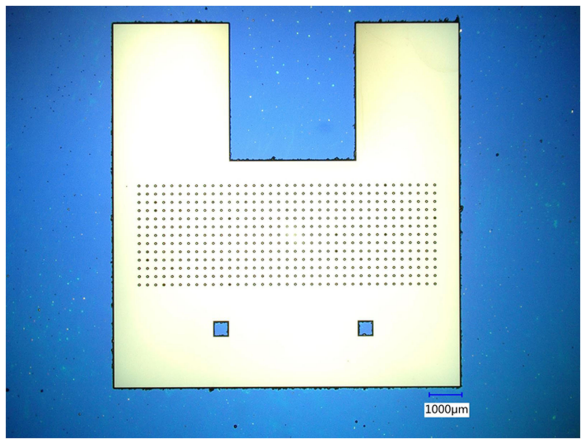

Fig. 16. Top view of a masked glass (blue) after etching the cavity. An array of 13 × 37 TGVs was made inside the cavity to interconnect the top and bottom side of the glass substrate.

TGVs providing power and ground to the ASIC and optical transceivers. The single layer provides simpler fabrication and assembly compared to 2.5D silicon interposer on an organic substrate or embedded multi-die interconnect bridge configurations [20] so has the potential for lower overall packaging cost. Glass substrates formed by a fusion draw process inherently have exceptional surface smoothness and the necessary flatness and dimensional stability for small line and space RDLs of tight geometric control, comparable to silicon and far better than organic substrates [21–22]. Yet unlike silicon, it can be formed in large formats that contain a high number of package substrates for cost effective, panel-level processing. Glass has a much higher Young's modulus (e.g., ~74 GPa) and hence stiffness than organic materials, and a coefficient of thermal expansion (CTE) that can be adjusted (e.g., 3…8 ppm/C) to match that of silicon or between silicon's CTE and that of a PCB. This provides a package substrate capable of obtaining low assembly warpage and improved solder joint fatigue life. The result of which is high assembly yields and high-power cycling reliability.

TGVs were formed in alkali-glass wafers in which optical interconnects are integrated by ion-exchange. Fig. 15 shows a cross-section view of a TGV array with entrance opening of 100 microns in 0.6 mm glass.

The mobility of ions in alkali-containing glasses can cause reliability issues. A different alkali glass was studied in previous work and compared to alkali-free glass. The leakage current

between isolated structures was tested before and after 96 hours of biased highly accelerated stress testing (HAST). The results indicate that for the alkali-glass substrate, a barrier layer is necessary between the substrate and Cu metallization to prevent Cu migration [23].

Providing a cavity on single side of the packaging substrate is key for surface mounting and evanescent coupling of photonic components. IOX waveguides are located underneath the glass top surface. The RDL and electrical bumps are inside the cavity to minimize the distance [Fig. 12(a)] between PIC evanescent couplers and IOX waveguides. The cavity was made by etching 50 microns into the glass to allow enough clearance underneath for the RDL and the electrical bumps. Fig. 16 shows the top view of on array of 481 TGV's. Fabrication of cavity occurs during the same process as the TGV's.

VI. Conclusion

Glass substrates with integrated optical waveguides, electrical interconnects and mechanical alignment features were introduced as a novel assembly platform for surface-mount photonic packaging. Low-loss single-mode optical waveguides were integrated in alkali-glass by silver-ion exchange. Waveguide propagation loss is less 0.1 dB/cm and coupling loss to single-mode fiber is 0.3 dB at 1310 nm wavelength. A fiber array connector interface was demonstrated by assembly of MTP-16 guide pins on mechanical passive alignment features in glass resulting in an average connector loss of 0.68 dB. Evanescent couplers were designed with coupling loss of <1 dB for TE/TM modes. TGVs and cavities were made in the same glass composition as the optical waveguides to evaluate process compatibility. The TGVs have an opening width of 100 microns in 0.6 mm glass thickness. Cavities were made with depth of 50 microns for the electrical interconnect. The presented use of glass IOX waveguides acts as an intermediary between a connector fiber pitch of 250 μm and a much more compact waveguide pitch. The utility of this approach is that it recovers valuable die real estate and allows for both electrical and optical routing on a single substrate. Multi-chip modules continue to be important for cost effective yield rates (reduced defect rate for smaller sized die), thermal separation of thermal sensitive PICs, and for separation of foundry processes (different materials, multiple process nodes) [24]. These results demonstrate the feasibility of integrating the key building blocks for a novel optoelectronic glass substrate for use in co-packaged optics in next-generation datacenters.

Acknowledgements

The authors would like to thank Jeffery S. Clark, Daniel W. Levesque, Barry J. Paddock and Katerina Rousseva for their assistance with processing glass wafers, connector assembly, and waveguide characterization.

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